The applicants do not concede this conclusion this reasoning. However, to speed prosecution of the present case, the applicants have amended claim 1 to include the phrase, "wherein said probe lines comprise strings of storage elements providing signal paths between said probe points and said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates," and claim 10 to include the phrase, "wherein said probe lines comprise strings of storage elements providing signal paths between said probe points and said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates," to better describe the applicants' probe lines.

Claims 1 and 10 refer to probe lines with the ability to move sets of system operation signals at system operation clock rates. Furthermore, the term, "sets of," describes a feature of the applicants' invention that each probe line can carry not only a single, but a set of system operation signals such that "sets of" system operation signals are stored in the claimed memory and that "sets of" system operation signals are retrievable.

Furthermore, the storage elements referred to in amended claims 1 and 10 refer to Probe Storage Element (PSE) elements 1000 shown in Figure 11. The PSE enables the reliable movement of the sampled system operation signals from the probe points to the memory even under conditions where the sample rate is faster than the speed at which a signal can be moved along a wire between the probe point and the memory. This is possible because during each clock cycle the system operation signals are staged and need only travel between successive Probe Storage Elements rather than traveling the entire distance between the probe points and the memory. By breaking a longer distance into several shorter segments which are linked by the PSEs, sets of said system operation signals are staged at multiple points along the probe lines. As taught by the applicants, the number of PSEs used for staging can be different for different probe lines and offline processing can be used to align data captured at the probe points.

For the ordinary testing of integrated circuits, test results may be captured at very slow rates to allow sufficient time for transfer of signals along the probe lines. This is not possible when target system is enabled to perform its system operations at normal system clock rates. Neither the Rajski *et al.* and Chandra *et al.* patents disclose probe line storage elements

as claimed by the applicants. The teachings provided by these references are not adequate to allow the capture of sequences of system operation signals that result from operating the system at high clock frequency rates in the system's normal operation.

Furthermore, the claimed storage elements along the probe lines enables the staging of the system operation signals along the probe lines and the time-multiplexing of each probe line among multiple system operation signals. This allows the probe lines to carry sets of system operation signals which are stored in the memory for subsequent analysis. By contrast, the teachings of Rajski *et al.* and Chandra *et al.* provide for carrying only a single value on each probe line at each clock cycle.

A perusal of the cited references illuminates the differences between the applicants' claimed invention and the references and, in particular, the limitations of the teachings of the references. For example, the Rajski patent teaches a built in self-test, which operates much slower than normal system operation as the applicants teach. Rajski *et al.* describes their Fig. 1 as "an exemplary IC incorporated with the teachings of the present invention". Referring to Rajski's Fig. 1, the Scan Registers 16 must be loaded and unloaded via the test port 20. Unlike the applicants "string of storage elements" which carry multiple cycles' worth of a single probe point's data, each flip-flop in the Rajski scan chain contains a different signal from the CUT (Circuits Under Test) 14. See Fig.1. This takes many clock cycles to load and unload for each cycle of CUT operation, and therefore can not be done during normal system operation. Likewise, the Chandra patent teaches a test point array with control-sense lines 34(typ) (see Fig. 2), which would have excessive loading of multiple transistors 36(typ) and no guarantee of meeting normal system operating clock frequencies under any expected implementations. The applicants point that the teachings of Chandra *et al.* do not result in the ability to sense the responses of normal operations in the test point array 14 of Fig. 1, unless the array was quite small. A typical example of a modern integrated circuit might have 40,000 registers within the test point array. This results in as many as 200 of the control-sense lines 34(typ), each with as many as 200 of the transistor loads 36(typ) on each control-sense line. Modern system clock frequencies in excess of 250 MHz are simply too high to drive such heavily loaded lines. The large capacitance on the line would filter such

high frequency signals making their capture by the control-sense receivers 17 in Fig. 1 impossible.

In the Office Communication dated April 4, 2001, the Examiner further stated, "Rajski teaches the invention substantially as claimed,....said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed to said integrated circuit." The applicants respectfully disagree. The Rajski patent specifically states the test port 20 (see Fig. 1) is a " register for interfacing between the embedded processor core and the multiple scan chains." (4th paragraph of the Summary). Furthermore, the non-volatile memory 18 can not be written into by the logic in Figure 1. As a result, there is no contemplation of storage sets of system operation signals for later retrieval.

The Examiner also stated, "Chandra teaches an integrated circuit having comprising a control unit..., a memory..., and a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points of said logic blocks...." Actually Chandra teaches a data register 22 (see Fig. 1), not a memory and further states, "According to the preferred embodiment, the data register 22 is a linear feedback shift register which is programmed to 'exclusively OR' the current register contents with parallel data input from one or more sense line receivers...(col. 5, lines10 – 15)." Such a "memory" would store system operation signals in such a way that they would not be individually retrievable as recited in claim 1, and therefore multiple system operation signals would not be retrieved as recited in claim 10.

Thus, the applicants respectfully request that amended independent claims 1 and 10 be granted. Dependent claims 2-9, 19-22, and 11-14 should be patentable given the patentability of these independent claims as argued above.

Independent claim 15 has been amended to include the word, "normal," with respect to system operations, and the word, "system," to clock signal rates. Furthermore, the phrase, "and carry" was added to the phrase, "enabling said probe lines responsive to said control unit to capture and carry sets of system operation signals of said logic blocks," to further describe the applicants' invention with greater specificity..

With respect to claim 15, the Examiner stated, "Mori teaches a test facilitating circuit of microprocessor including loading and retrieving operations performing at one or

more clock signal rates internal to said integrated circuit." The applicants argue that is all Mori teaches is a test of a microprocessor. In fact, the Examiner further states of Mori, "After the test, an external tester reads the test results out of the cache memory and examines them...." In contrast, claim 15 specifically recites, "an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines...". The memory is specifically recited as separate from the logic blocks to better describe, in part, that normal operation of the blocks can be performed while the memory is being loaded with the normal system operation signals. This can not be done with Mori, which teaches using the cache, a functional part of a processor, to test the processor while in test mode. Clearly, the processor can not perform normal operations while the cache is being used for test, as required of the memory in claim 15.

Furthermore, the Examiner claims, "It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski to provide a built in self test circuitry including a facilitating circuit taught by Mori...." The applicants submit that such a circuit could indeed load, retrieve, and store TEST operations at one or more clock signal rates, but neither Rajski et al. nor Mori contemplate operating their logic for test during normal system operation. The Chandra patent doesn't preserve the captured data. As such, a design using such a combination of Rajski, Mori and Chandra would not function during normal system operation of said blocks, as claim 15 recites.

Amended claim 15 recites capturing, storing and retrieving "sets of" system operation signals. The probe lines "capture and carry sets of system operation signals." The "capture and carry" is made possible by the use of probe storage elements, as noted above. This teaching is absent in the Mori, Chandra or Rajski patents. The Examiner states that, "It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski and Chandra to include a facilitating circuit taught by Mori for loading and retrieving operations at one or more clock signals rates internal to integrated circuit. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide an efficient method of testing a high frequency integrated circuit using an inexpensive tester [see Mori col, 1 lines 6-11 and col. 1 line 61- col. 2 line 10]."

The applicants respectfully disagree with this conclusion. As argued above, Rajski *et al.* or Chandra *et al.* have been concerned about capturing test results at very slow rates in order to allow sufficient time for transfer of signals along the probe lines. This is not possible when the target system has been enabled to perform its system operations at normal system clock rates. Thus, the teachings provided by Rajski *et al.* or Chandra *et al.* do not address this problem. The invention recited in amended claim 15 would not have been obvious to skilled persons focusing on the problem of testing an integrated circuit by means of using probe lines. The Rajski *et al.* or Chandra *et al.* patents would teach them to adjust the test speed and slow the circuit to eliminate the timing problem during testing. This is especially true if the skilled person is motivated to use an inexpensive tester, as the Examiner argues.

Thus, the applicants respectfully request that claim 15 be granted. Furthermore, claims 16-18 should also be granted for at least being dependent upon allowable subject matter.

Finally, the applicants submit herewith U.S. Patent No. 6,182,247, which issued January 20, 2001 to A.I. Hermann *et al.* This reference describes on-chip logic analysis. See, for example, Fig. 5 and the specification referring to a base configuration of an embedded logic analyzer 260. Fig. 6 shows the logic analyzer 260, which has an interface 262 to monitor signals internal to the PLD 16, a memory 342, and an external interface 264. In a perusal of this reference, the applicants have not been able to find a teaching of probe storage elements as recited in independent claims 1, 10 and 15. The applicants' invention as recited in these claims is patentably distinguishable over the Hermann *et al.* patent.

Therefore, in view of the amendments above and remarks thereto, the applicants respectfully request that the rejections be removed, that claims 1-22 be allowed and the case be passed to issue.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at (650) 564-9888.

Respectfully submitted,

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